**In the Claims**:

Claims 1-30 (CANCELLED)

31. (CURRENTLY AMENDED) An integrated circuit for use with a dual-mode smart card and configurable in a first and second mode of operation comprising:

a ~~microprocessor~~ processor;

a switching block connected to said ~~microprocessor~~ processor; and

an external interface connected to said switching block and comprising a first port configurable for communicating in a first mode of operation when a first mode of operation is detected and a second port configurable for communicating in a second mode of operation when a second mode of operation is detected, wherein said ~~microprocessor~~ processor and switching block configure the first port to allow debugging and/or software development through the first port and allow debugging and/or software development through the second port.

32. (CURRENTLY AMENDED) An integrated circuit according to Claim 31, wherein said ~~microprocessor~~ processor and switching block configure the first port to allow debugging and/or software development through the first port in the second mode of operation and allow debugging and/or software development through the second port in the first mode of operation.

33. (ORIGINAL) An integrated circuit according to Claim 31, wherein said first mode of operation comprises an ISO mode

of operation in accordance with the International Standards Organization protocol.

34. (ORIGINAL) An integrated circuit according to Claim 33, wherein said ISO mode of operation comprises an ISO mode of operation in accordance with the International Standards Organization 7816 (ISO 7816) protocol.

35. (ORIGINAL) An integrated circuit according to Claim 31, wherein said second mode of operation comprises a USB mode of operation and said second port comprises a USB port.

36. (ORIGINAL) An integrated circuit according to Claim 31, wherein said first port comprises a serial interface.

37. (ORIGINAL) An integrated circuit according to Claim 31, and further comprising a dual-mode configuration circuit connected to the switching block for configuring the integrated circuit in one of the first or second modes of operation.

38. (ORIGINAL) An integrated circuit according to Claim 37, wherein said dual-mode configuration circuit detects a first mode of operation or second mode of operation upon a power-on-reset.

39. (ORIGINAL) An integrated circuit according to Claim 31, wherein said first port comprises an I/O contact through which debugging and/or software development occurs when configured in a second mode of operation.

40. (ORIGINAL) An integrated circuit according to Claim 31, wherein first port comprises reset and clock contacts.

41. (ORIGINAL) An integrated circuit according to Claim 31, and further comprising a circuit for disabling one of the first or second ports used for debugging and/or software development after debugging and/or software development is completed.

42. (CURRENTLY AMENDED) A dual-mode smart card configurable in both a first and second mode of operation comprising:

a card body;

a dual-mode integrated circuit carried by said card body and comprising,

a ~~microprocessor~~ processor,

a switching block connected to said ~~microprocessor~~ processor, and

an external interface connected to said switching block and comprising a first port configurable for communicating in a first mode of operation when a first mode of operation is detected and a second port configurable for communicating in a second mode of operation when a second mode of operation is detected, wherein said ~~microprocessor~~ processor and switching block configure the first port to allow debugging and/or software development through the first port and allow debugging and/or software development through the second port.

43. (CURRENTLY AMENDED) A dual-mode smart card according to Claim 42, wherein said ~~microprocessor~~ processor and switching block configure the first port to allow debugging and/or software development through the first port in the second mode of operation and allow debugging and/or software development through the second port in the first mode of operation.

44. (ORIGINAL) A dual-mode smart card according to Claim 42 wherein said first mode of operation comprises an ISO mode of operation in accordance with the International Standards Organization protocol.

45. (ORIGINAL) A dual-mode smart card according to Claim 44, wherein said ISO mode of operation comprises an ISO mode of operation in accordance with the International Standards Organization 7816 (ISO 7816) protocol.

46. (ORIGINAL) A dual-mode smart card according to Claim 42, wherein said second mode of operation comprises a USB mode of operation and said second port comprises a USB port.

47. (ORIGINAL) A dual-mode smart card according to Claim 42, wherein said first port comprises a serial interface.

48. (ORIGINAL) A dual-mode smart card according to Claim 42, and further comprising dual-mode configuration

circuit connected to the switching block for configuring the integrated circuit in one of the first or second modes of operation.

49. (ORIGINAL) A dual-mode smart card according to Claim 48, wherein said dual-mode configuration circuit detects a first mode of operation or second mode of operation upon a power-on-reset.

50. (ORIGINAL) A dual-mode smart card according to Claim 42, wherein said first port comprises an I/O contact through which debugging and/or software development occurs when configured in a second mode of operation.

51. (ORIGINAL) A dual-mode smart card according to Claim 42, wherein first port comprises reset and clock contacts.

52. (ORIGINAL) A dual-mode smart card according to Claim 42, and further comprising a circuit for disabling one of the first or second ports used for debugging and/or software development after debugging and/or software development is completed.

53. (ORIGINAL) A method of operating an integrated circuit for use with a dual-mode smart card and configurable in a first and second mode of operation comprising the steps of:

detecting first or second modes of operation; and

configuring the integrated circuit for communicating

through first or second ports in respective first or second modes of operation and debugging and/or software development through the first port when a second mode of operation is detected and debugging and/or software development through the second port when a first mode of operation is detected.

54. (ORIGINAL) A method according to Claim 53, wherein the first mode of operation comprises an ISO mode of operation in accordance with the International Standards Organization protocol.

55. (ORIGINAL) A method according to Claim 54, wherein said ISO mode of operation comprises an ISO mode of operation in accordance with the International Standards Organization 7816 (ISO 7816) protocol.

56. (ORIGINAL) A method according to Claim 53, wherein the second mode of operation comprises a USB mode of operation and the second port comprises a USB port.

57. (ORIGINAL) A method according to Claim 53, wherein the first port comprises a serial interface.

58. (ORIGINAL) A method according to Claim 53, and further comprising the step of debugging through a serial I/O contact of the first port when configured in the second mode.

59. (ORIGINAL) A method according to Claim 53, and further comprising the step of detecting a first or second mode of operation at a power-on-reset.

60. (ORIGINAL) A method according to Claim 53, and further comprising the step of disabling one of the first or second ports used for debugging and/or software development after debugging and/or software development is completed.